Your search matched **3** of **972916** documents.

A maximum of **3** results are displayed, **50** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((rtl simulator) and ((1950 <in> py) or (1951 <in> py) or Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A hardware/software co-simulation environment for micro-processor design with HDL simulator and OS interface**
Ito, Y.; Nakamura, Y.;
Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia and South Pacific , 28-31 Jan. 1997
Page(s): 377 -382

[Abstract] [PDF Full-Text (572 KB)] **IEEE CNF**

2 **A tampering protocol for reducing the coherence transactions in regular computation**
Takesue, M.;
Parallel Architectures, Algorithms, and Networks, 1997. (I-SPAN '97) Proceedings. Third International Symposium on , 18-20 Dec. 1997
Page(s): 465 -471

[Abstract] [PDF Full-Text (672 KB)] **IEEE CNF**

3 **Bit map control processor (BMCP) design**
Sumi, M.; Kai, N.; Tanaka, S.; Minagawa, T.; Nagashima, I.; Hamai, T.; Mori, J.;
Custom Integrated Circuits Conference, 1988., Proceedings of the IEEE 1988 , 16-19 May 1988
Page(s): 8.6/1 -8.6/7

[Abstract] [PDF Full-Text (516 KB)] **IEEE CNF**

Your search matched **2** of **972916** documents.

A maximum of **2** results are displayed, **50** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((rtl and (vhdl or verilog) and cycle accurate) and ((1950 Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Cycle and phase accurate DSP modeling and integration for HW/SW co-verification**
Guerra, L.; Fitzner, J.; Talukdar, D.; Schlager, C.; Tabbara, B.; Zivojnovic, V.;
Design Automation Conference, 1999. Proceedings. 36th , 21-25 June 1999
Page(s): 964 -969

[Abstract] [PDF Full-Text (628 KB)] **IEEE CNF**

2 **Fast hardware-software co-simulation using VHDL models**
Tabbara, B.; Sgroi, M.; Sangiovanni-Vincentelli, A.; Filippi, E.; Lavagno, L.;
Design, Automation and Test in Europe Conference and Exhibition 1999. Proceedings , 9-12 March 1999
Page(s): 309 -316

[Abstract] [PDF Full-Text (652 KB)] **IEEE CNF**

Search Results

Search Results for: **[(cycle accurate simulator)<AND>(meta_published_date <= 05-01-1999)]**
Found **15** of **121,350 searched.**

Search within Results

GO > Advanced Search > Search Help/Tips

Sort by: Title Publication Publication Date Score Binder

Results 1 - 15 of 15 short listing

1 Improving the performance of speculatively parallel applications on the Hydra CMP 82%
Kunle Olukotun , Lance Hammond , Mark Willey
Proceedings of the 13th international conference on Supercomputing May 1999

2 Design decisions influencing the UltraSPARC's instruction fetch architecture 80%
Robert Yung
Proceedings of the 29th annual ACM/IEEE international symposium on Microarchitecture December 1996
Designing a modern microprocessor is a complex task that demands careful balance between cycle time, cycle-per-instruction and area costs. In particular, the instruction fetch unit greatly affects the performance of a multi-issue processor. It must provide adequate bandwidth to sustain peak instruction issue rate and must predict future instruction sequences with high accuracy. In the UltraSPARC prefetch and dispatch unit design, we examined a technique that combined two prediction methods: pred ...

3 An intelligent memory system 77%
A. Asthana , H. V. Jagadish , J. A. Chandross , D. Lin , S. C. Knauer
ACM SIGARCH Computer Architecture News September 1988
Volume 16 Issue 4
SWIM(Structured Wafer-Scale Intelligent Memory) is a high bandwidth, multi-ported, disk-sized memory system capable of storing, maintaining, and manipulating data structures within it, independent of the main processing units. Up to thousands of active storage elements, each element having some storage and some associated processing logic, function independently or in groups to implement userdefined objects. SWIM increases memory functionality to better balance the time spent in moving data with ...

4 Maps: a compiler-managed memory system for raw machines 77%
Rajeev Barua , Walter Lee , Saman Amarasinghe , Anant Agarwal
ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture May 1999
Volume 27 Issue 2
This paper describes Maps, a compiler managed memory system for Raw architectures. Traditional processors for sequential programs maintain the abstraction of a unified memory by using a single centralized memory system. This implementation leads to the infamous "Von Neumann bottleneck," with machine performance limited by the large memory latency and limited memory bandwidth. A Raw architecture addresses this problem by taking advantage of the rapidly increasing transistor budget to move much of ...

5 Efficient management of memory hierarchies in embedded DRAM systems 77%
Ashley Saulsbury , Su-Jaen Huang , Fredrik Dahlgren
Proceedings of the 13th international conference on Supercomputing May 1999

6 Exploiting SIMD parallelism in DSP and multimedia algorithms using the AltiVec technology 77%
Huy Nguyen , Lizy Kurian John
Proceedings of the 13th international conference on Supercomputing May 1999

7 A bandwidth-efficient architecture for media processing 77%
Scott Rixner , William J. Dally , Ujval J. Kapasi , Brucek Khailany , Abelardo López-Lagunas , Peter R. Mattson , John D. Owens
Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture November 1998

8 Software performance engineering a digital signal processing application 77%
David P. Kelly , Robert S. Oshana
Proceedings of the first international workshop on Software and performance October 1998

9 Multi-level texture caching for 3D graphics hardware 77%
Michael Cox , Narendra Bhandari , Michael Shantz
ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture April 1998
Volume 26 Issue 3
Traditional graphics hardware architectures implement what we call the *push architecture* for texture mapping. Local memory is dedicated to the accelerator for fast local retrieval of texture during rasterization, and the application is responsible for managing this memory. The push architecture has a bandwidth advantage, but disadvantages of limited texture capacity, escalation of accelerator memory requirements (and therefore cost), and poor memory utilization. The push architecture also ...

10 The construction of a retargetable simulator for an architecture template 77%
Bart Kienhuis , Ed Deprettere , Kees Vissers , Pieter van der Wolf
Proceedings of the 6th international workshop on Hardware/software codesign March 1998

11 ProfileMe: hardware support for instruction-level profiling on out-of-order processors 77%
Jeffrey Dean , James E. Hicks , Carl A. Waldspurger , William E. Weihl , George Chrysos
Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture December 1997
Profile data is valuable for identifying performance bottlenecks and guiding optimizations. Periodic sampling of a processor's performance monitoring hardware is an effective, unobtrusive way to obtain detailed profiles. Unfortunately, existing hardware simply counts events, such as cache misses and branch mispredictions, and cannot accurately attribute these events to instructions, especially on out-of-order machines. We propose an alternative approach, called ProfileMe, that samples instructio ...

12 Prefetching in a texture cache architecture 77%
Homan Igehy , Matthew Eldridge , Kekoa Proudfoot
Proceedings of the 1998 EUROGRAPHICS/SIGGRAPH workshop on Graphics hardware August 1998

13 Talisman: commodity realtime 3D graphics for the PC 77%
Jay Torborg , James T. Kajiya
Proceedings of the 23rd annual conference on Computer graphics and interactive techniques August 1996

14 Operating system support for improving data locality on CC-NUMA compute servers 77%
Ben Verghese , Scott Devine , Anoop Gupta , Mendel Rosenblum
Proceedings of the seventh international conference on Architectural support for programming languages and operating systems September 1996
Volume 31 , 30 Issue 9 , 5
The dominant architecture for the next generation of shared-memory multiprocessors is CC-NUMA (cache-coherent non-uniform memory architecture). These machines are attractive as compute servers because they provide transparent access to local and remote memory. However, the access latency to remote memory is 3 to 5 times the latency to local memory. CC-NOW machines provide the benefits of cache coherence to networks of workstations, at the cost of even higher remote access latency. Given the larg ...

15 The M-Machine multicomputer 77%
Marco Fillo , Stephen W. Keckler , William J. Dally , Nicholas P. Carter , Andrew Chang , Yevgeny Gurevich , Whay S. Lee
Proceedings of the 28th annual international symposium on Microarchitecture December 1995

Results 1 - 15 of 15 **short listing**

Search Results

Nothing Found

Your search for the *Phrase* **(instruction accurate simulator)<AND>(meta_published_date <= 05-01-1999)** did not return any results.
To search for *terms* separate them with **AND** or **OR**.
Click on the suggested options:

(instruction AND accurate AND simulator)<AND>(meta_published_date AND <= AND 05-01-1999 AND)

(instruction OR accurate OR simulator)(meta_published_date OR <= OR 05-01-1999 OR)

To search for names try using only the last or first name.

You may revise it and try your search again below or click advanced search for more options.

(instruction accurate simulator) <AND>(meta_published_date <= 05-01-1999)

SEARCH [**Advanced Search**] [**Search Help/Tips**]

Complete Search Help and Tips

The following characters have specialized meaning:

Special Characters	Description
, ( ) [	These characters end a text token.
= > < !	These characters end a text token because they signify the start of a field operator. (! is special: != ends a token.)
` @ \Q < { [!	These characters signify the start of a delimited token. These are terminated by the end character associated with the start character.

Search Results

Search Results for: **[(rtl AND processor AND performance) AND (vhdl verilog)<AND>(meta_published_date <= 05-01-1999)]**
Found **2** of **121,350 searched.**

Search within Results

GO > Advanced Search > Search Help/Tips

Sort by: **Title** **Publication** **Publication Date** **Score** Binder

Results 1 - 2 of 2 **short listing**

1 High-level power modeling, estimation, and optimization 77%
Enrico Macii , Massoud Pedram , Fabio Somenzi
Proceedings of the 34th annual conference on Design automation conference June 1997

2 Basic concepts for an HDL reverse engineering tool-set 77%
Gunther Lehmann , Bernhard Wunder , Klaus D. Müller-Glaser
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997
Designer's productivity has become the key-factor of the development of electronic systems. An increasing application of design data reuse is widely recognized as a promising technique to master future design complexities. Since the intellectual property of a design is more and more kept in software-like hardware description languages (HDL), successful reuse depends on the availability of suitable HDL reverse engineering tools. This paper introduces new concepts for an integrated HDL reverse eng ...

Results 1 - 2 of 2 **short listing**

CiteSeer Find: instruction accurate simulator Documents Citations

Searching for **PHRASE instruction accurate simulator**.
Restrict to: Header Title Order by: Citations Hubs Usage Date Try: Amazon B&N Google (RI) Google (Web) CSB DBLP
Order: citations weighted by year.

Using a Soft Core in a SoC Design: Experiences with.. - Dey, Panigrahi, Chen.. (2000) (Correct)
3Th verification support includes an **instruction-accurate simulator** (22,454 lines of C code)Verilog
esdat.ucsd.edu/~lichen/esdat/paper/DnT_final.pdf

Try your query at: Amazon Barnes & Noble Google (RI) Google (Web) CSB DBLP

CiteSeer Find: cycle accurate simulator and rtl Documents Citations

Searching for **cycle accurate simulator and rtl**.
Restrict to: Header Title Order by: Citations Hubs Usage Date Try: Amazon B&N Google (RI) Google (Web) CSB DBLP
3 documents found. **Order: citations weighted by year.**

The Construction of a Retargetable Simulator for an.. - Bart Kienhuis Ed (1998) (Correct) (4 citations)
set simulator, 40,000 for a clock-**cycle accurate simulator** and 500 for an **RTL** accurate simulator
for a clock-**cycle accurate simulator** and 500 for an **RTL** accurate simulator in VHDL. Simulating, for
as C functions within the PAMELA run-time library (**RTL**)This is a multithreading package that performs
ptolemy.eecs.berkeley.edu/~kienhuis/ftp/codes98.pdf

A High-Level Hardware Design Methodology using C++ - Roth, Ramanathan (1999) (Correct)
Furthermore, our class library provides a **cycle-accurate simulator** that enables creation of cycle wrapped
designs from a purely functional level to low level **RTL** while remaining in a single unified design
as Verilog and VHDL were initially centered around **RTL** designs. Higher levels of abstraction were more
www.ics.uci.edu/~dinesh/pubs/hldvt99.ps.Z

A Method to Construct Reconfigurable Simulators from.. - Bart Kienhuis (1997) (Correct)
the SPIM simulator in table I, the clock-**cycle accurate simulator** tmsim is given. Going down level in
CClock-Cycle 10.000 3.6 Hrs (dataflow) Dlx Vhdl **Rtl** 500 30 Days (dlx) A Processor Simulator (e.g.
paper. If we go down one more level in accuracy, the **RTL** level simulator DLX is given that has a factor 200
www.stw.nl/prorisc/workshop/proc/psz/kienhuis.ps.gz

Try your query at: Amazon Barnes & Noble Google (RI) Google (Web) CSB DBLP

CiteSeer Find: processor and performance and simu Documents Citations

Searching for **processor and performance and simulator and rtl**.
Restrict to: Header Title Order by: Citations Hubs Usage Date Try: Amazon B&N Google (RI) Google (Web) CSB DBLP
11 documents found. **Order: citations weighted by year.**

Compiler-directed Data Prefetching in Multiprocessors with.. - Edward Gornish (1990) (Correct) (68 citations)
bandwidth in the interconnection between the **processors** and the memories, coupled with long delays
by using static analysis to estimate the **performance** improvement afforded by our prefetching
realistic shared-memory system using an **RTL**-level **simulator** and real codes. This differs from previous
www.csrd.uiuc.edu/reports/949.ps.gz

One or more of the query terms is very common - only partial results have been returned. Try Google (RI).

Instruction Selection, Resource Allocation, and Scheduling in .. - Hanono, Devadas (1998) (Correct) (3 citations)
produces optimized machine code for target **processors** with different instruction set architectures.
thus allows us to accurately evaluate the **performance** of different architectures on application
system is evaluated using a hardware-software co-**simulator**. The partitioning and **processor** design are
glen.lcs.mit.edu/~devadas/pubs/aviv.ps

Automatic Generation of Microarchitecture Simulators - Önder, Gupta (1998) (Correct) (2 citations)
three **simulators** ranging from simple pipelined **processors** to complicated out-of-order issue **processors**
studies are carried out to estimate the expected **performance** of the microarchitecture on a variety of
Automatic Generation of Microarchitecture **Simulators** Soner Onder Rajiv Gupta Department of
www.cs.pitt.edu/~soner/publications/iccl98.ps

Application-driven Design Automation for Microprocessor Design - Iksoo Pyo (1992) (Correct) (2 citations)
design space and synthesize a single chip VLSI **processor** from a high-level specification of the
used to motivate design decisions and optimize **performance**. Compiler optimizations are considered during
consists of a Semantic Design Generator (SDG)a **simulator**, an evaluator, a translator, a design library,
www.isi.edu/acal/tech-reports/1992/tr-92-03.ps.Z

A Design Experience of A GaAs Datapath Generation Using.. - Moussa, GUYOT (Correct)
like microprocessors or Digital Signal **Processor** (DSP) circuits. In this way the designer can
onto a GaAs technology library to achieve high **performance** regarding speed, area and power consumption.
Transistor level Timing verification HSPICE **Simulator** Place and route return to the source file No!
verdon.imag.fr/pub/ISD/postscript/icm95.ps.gz

Execution-Driven Distributed Simulation of Parallel.. - Ricciulli, Lincoln.. (Correct)
of the latency and throughput of the inter-**processor** interconnection network. In the experiments we
{livio, lincoln, meseguer}csl.sri.com Keywords: **Performance** evaluation, Distributed simulation of computer
distributed event causality relations. The **simulator** correctly executes a given parallel application
www.csl.sri.com/reports/postscript/sri-csl-95-05.ps.Z

Synthesis of TTL Specification: A Case Study - Carchiolo, Malgeri, Mangioni (Correct)
an architecture including a single generalpurpose **processor**, a few application-specific hardware components
Project "Design Methodologies and Tools of High **Performance** Systems for Distributed Applications" power
tested. The Formal Tools block also comprises a **simulator** which is used during specification and the
www.cdc.unict.it/~carchiol/articoli-mosaico/Cesa98.ps

EEL: Machine-Independent. . . - Larus, al. (1995) (Correct)
computer from the logical cycle times of **processors** directly executing a parallel program. The
fault isolation, architecture translation, **performance** measurement, simulation, and optimization
example, the Wisconsin Wind Tunnel architecture **simulator** [19] drives a distributed, discrete-event
ftp.cs.wisc.edu/wwt/pldi95_eel.ps

Inter-Domain Movement of Functionality as a Repartitioning.. - Stoy, Peng (1995) (Correct)
implementation is considered as a specialized co-**processor** which will be controlled by and interact with

new versions of a product to offer other cost/**performance** trade-offs. One obvious way to achieve (Re-Partitioning Transformation/ Optimization **Simulator** Fig. 2 Design environment. 3 -tasks such ftp.ida.liu.se/pub/labs/cadlab/reports/r-95-33.ps.gz

Evaluation of Design Error Models for Verification Testing.. - Van Campenhout, al. (Correct)
instruction set architecture (ISA) model of the **processor**. Both models are assumed to be executable. A is an essential activity in the design of high-**performance** microprocessors, especially for concluding remarks are given in Section 5. **RTL simulator** Specification **simulator** Equal? Diagnose & www.eecs.umich.edu/~tnm/papers/mtv98.ps

Towards a Unified Analysis Methodology of HW/SW Systems based.. - Castillo, al. (Correct)
which can be quite complex themselves (e.g.**processor** cores, microcontrollers, floating point and block consists of a HW-part and a SW-part, the **performance** of such a BB is determined by the HW debugging features are provided by the ASM **simulator**. In this paper, after a short overview of some ftp.eecs.umich.edu/groups/gasm/hwswmodel.ps.gz